Towards real-time digital pulse process algorithms for CsI(Tl) detector array at External Target Facility in HIRFL-CSR*

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A fully digital data acquisition system based on a field-programmable gate array (FPGA) was developed for a CsI(Tl) array at the External Target Facility (ETF)in the Heavy Ion Research Facility in Lanzhou(HIRFL). To process the CsI(Tl) signals generated by γ-rays and light-charged ions, a scheme for digital pulse processing algorithms is proposed. Every step in the algorithms was benchmarked using standard γ and α sources. The scheme, which included a moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution and digital charge comparison was subsequently implemented on the FPGA. A good energy resolution of 5.7% for 1.33 MeV γ rays and excellent α-γ identification using the digital charge comparison method were achieved, which satisfies CsI(Tl) array performance requirements.

Keywords: CsI(Tl) array, on-line digital algorithms, moving average filter, moving window deconvolution, on-line particle identification algorithms

I. INTRODUCTION

The structure of atomic nuclei near drip lines is one of the most fascinating fields for nuclear physicists, and has continuously attracted researchers to build large facilities for experimental studies [1, 2]. One such facility is the External Target Facility(ETF) at the Heavy Ion Research Facility in Lanzhou(HIRFL) [3]. The ETF is a large integrated experimental platform for nuclear physics research. It comprises several detector systems and can provide complete kinematic measurements of nuclear reactions at intermediate and high energies [3–7]. The CsI(Tl) array, consisting of 1024 CsI(Tl) detectors, is one of the most important detector systems in the ETF. It can measure γ-rays up to 10 MeV in the center-of-mass(CM) frame [8]. Such a design, an inorganic scintillation array with high granularity, is also used in many detector arrays, such as DALI2 at RIKEN [9, 10] and CALIFA at FAIR [11, 12], and it enables a relatively good energy resolution of the γ-rays to be obtained owing to its good angular resolution [10].

In combination with silicon strip detectors, the CsI(Tl) array at the ETF can also be used to measure light-charged particles. However, the energy loss of light-charged particles in CsI(Tl) crystals is several tens of times greater than that of γ-rays. To satisfy the highly dynamic requirements of the measurements, the electronic system was updated. High-granularity detectors require highly integrated electronic systems [13–16]. The traditional solution, also known as the previous scheme of the CsI(Tl) array, uses application-specific integrated circuit (ASIC) chips for signal processing [17]. However, these chips are highly customized and it is difficult to extend their functionality. Waveform digitization based on flash analog-to-digital converters (ADC) has been developed for over two decades. The analog signals extracted from the detector or charge sensitive amplifier (CSA) are directly digitized. Therefore, a minimal loss of signal information can be achieved using a much simpler circuit. Other advantages include a higher sustained count rate, flexibility through a variety of digital pulse process (DPP) algorithms, and compact structures, which facilitate the development of a highly integrated system. Owing to these aforementioned advantages, a fully digital technique was chosen as the solution for a new measurement system for the CsI(Tl) array.

However, this scheme has one drawback. The digitization of the entire waveform means that a significant amount of data must be read. For a one-channel signal digitized by a 14-bit flash ADC with a sampling frequency of 50 MS/s, the data rate was approximately 83.4 MByte/s. When this flash ADC is used for the CsI(Tl) array at the ETF, the amount of data is extremely large, and the transmission bandwidth of the Data Acquisition (DAQ) system may be overloaded. Zero suppression should be performed after wave digitization to reduce data transmission pressure. Using DPP algorithms in the onboard field-programmable gate array (FPGA) to extract specific waveform information, such as the amplitude and arrival time, the entire amount of waveform sampling data can be reduced to a few physical quantities, further reducing the data volume. Moreover, owing to conflicts between the FPGA limited computational resources and the large number of detector channels, the new electronic system may require a compromise in precision with somewhat uncomplicated DPP algorithms, and these algorithms are the focus of this study.

The remainder of this paper is organized as follows: Section II concentrates on general considerations regarding which procedures should be executed in the FPGA and in what order. Section III lists the specific DPP algorithms for each procedure and discusses the rationale for algorithm se-

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lection through bench testing. Section IV presents the final DPP algorithms scheme in the FPGA and discusses their performance after implementing all the algorithms in the FPGA. Section V summarizes the study findings with an outline of future research directions.

II. GENERAL CONSIDERATION OF DPP ALGORITHMS

In nuclear physics, signals from detectors are completely random. This indicates that DPPs for the CsI(Tl) array should perform well in the time domain [18]. As a calorimeter, the critical physical quantity measured by the CsI(Tl) array is the energy of the incident gamma rays or light ions. Thus, the method for obtaining energy information from the recorded waveform of the detector is the most critical aspect of this study, and energy resolution is a key criterion for DPP algorithms. Further algorithms such as a smooth filter and baseline recovery were used to achieve a good Signal to Noise Ratio (SNR) value and energy resolution. The signal arrival-time information is responsible for generating a system trigger. It also helps to reduce the background noise by selecting appropriate time windows for off-line data analysis [19].

CsI(Tl) crystal has been used for many years to identify light ions and gamma rays using pulse-shape analysis. This is because the responses of the CsI(Tl) crystal vary with different types of particles, resulting in different waveform shapes being generated by the CsI(Tl) detector [20–24]. In the case of a CsI(Tl) array with high spatial coverage and large granularity, the gamma rays and light ions can strike different elements of the detector simultaneously and form different hit clusters. When the energy spectrum is reconstructed by some algorithms, such as the add-back technique, the spectrum between the charged particles and the gamma rays may be superimposed. Thus, clear separation of the gamma rays and charged particles can result in a good gamma energy spectrum with a lower background of charged particles. Pulse-shape analysis can improve the performance of particle identification(PID) compared to the traditional ΔE-E method [25]. In some situations, when the atomic number Z of the measured ions is less than four, pulse shape analysis can also help simplify the detector setup because the CsI(Tl) detector can perform identification by itself [26–28]. Considering the aforementioned advantages, on-line algorithms for pulse shape analysis are also in demand.

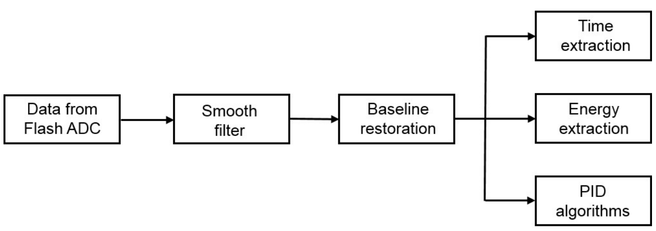

Fig. 1. DPPs in FPGA for the CsI(Tl) array of ETF.

Overall, In this study, DPP algorithms are organized in the FPGA in the manner shown in Figure 1. The final outputs were the arrival time, energy, and quantities representing the incident particles PID results. Each process as shown in Figure 1 is described in detail in the following sections.

III. ALGORITHMS SELECTIONS WITH OFF-LINE ANALYSIS

To identify suitable algorithms for each process shown in Figure 1, a test bench including an element of CsI(Tl) array and the DAQ system was set up. The DAQ system is an intermediate development product of the CsI(Tl) array that contains a CSA module and a DAQ board. A 14 bit flash ADC with a sampling rate of 50 MS/s was embedded in the DAQ board to digitize the signal from the CSA module. The DAQ board can be operated in two modes: raw waveform mode, in which the Flash ADC data are recorded directly into PC memory, and algorithm mode, in which the data are processed by algorithms in FPGA with only the results recorded. Because the DPP algorithms are not specified, the test bench is operated in the raw waveform mode to select the appropriate algorithms for the CsI(Tl) array. The criteria for selecting suitable algorithms are based on the tradeoff between performance, FPGA source consumption, and execution speed. The Flash ADC sampling rate was set to 25 Ms/s in the FPGA because the data volume was too large for the raw waveform mode.

A. Smooth filter

Because the detector signals are always distorted by random noise, the goal of this procedure is to reduce the high-frequency noise while not significantly changing the detector signals to preserve the signal characteristics and improve the data SNR. This procedure was performed initially because it may slightly alter the raw waveform and affect the performance of the other procedures.

The moving average filter (MAF) is the most commonly used smooth filter in the time domain owing to its simplicity, ease of implementation, and rapid execution speed. In addition to the aforementioned advantages, it offers the lowest noise for a given edge sharpness for any linear filter [18]. Other optional filters include the Savitzky–Golay [29], binomial [28, 30], Whittaker [31], and the Kalman filters [32, 33]. Although these smooth filters perform well in multiple fields such as Raman and Mössbauer spectroscopy, complex algorithms make them difficult to implement in the FPGA. For this reason, the MAF was chosen as a smooth filter for the CsI(Tl) array.

The only parameter for MAF is the number of samples averaged over. Its value should be chosen with care because as the value increases, the noise decreases, while the edges become less sharp. The aforementioned test bench, which was operated using cosmic rays, was used to acquire raw waveform data, and the MAF algorithms were executed with different parameter values in the off-line analysis. The results are presented in Figure 2. The reason for using a power of two for the parameter values is that the division is simpler to

implement in the FPGA using only shift operations. Finally, owing to its good performance in high-frequency noise reduction and small waveform changes, the value of the parameter was set as equal to 8.

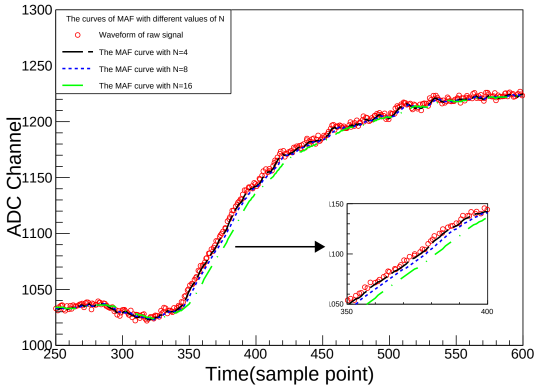

Fig. 2. (Color online) Comparison among MAF results with different values of N. Inset illustrates leading edges in the picture.

B. Baseline restoration

In many cases, the baseline is assumed constant at all times. This enabled the baseline value to be measured at any time while the DAQ system was idle during the experiment. However, this assumption is only true when the signal length is short and the count rate is relatively low. This is certainly not the case in this instance, because the CSA signal extracted has a long tail. A good solution is to use optimal filters [34]. However, complicated arithmetic discourages us from proceeding further. To simplify the procedure, it was assumed that the baseline remained constant within each selected dataset, which contained only one signal waveform with several baseline data points in front. This baseline data can subsequently be used to calculate the baseline value of each individual event. Reference [35] showed that two values, the average and median of the baseline data, can be used to evaluate the baseline level. The method for obtaining average baseline data is clear. The median is the exact quantity in the middle of the baseline dataset when ordered. Reference [35] showed that the median is a better estimate of the baseline level than the average over a wide range of count rate loads. The other two methods, which are called "averaging over the selection set" and "averaging over the flat chunk selection set" respectively, are also introduced in [35]. These two methods are identical in terms of how to proceed, albeit differ in terms of data selection. Further detail regarding both methods can be found in [35], and the main procedures are summarized in the flowchart shown in Figure 3. Over a wide range of count rate loads, these two methods provide better estimates of the baseline than either the average or the median alone. In this case, because the baseline dataset has already been selected, the procedure list in Figure 3 can be processed directly. Therefore, both methods are treated as a single method and are hereafter called iterative methods.

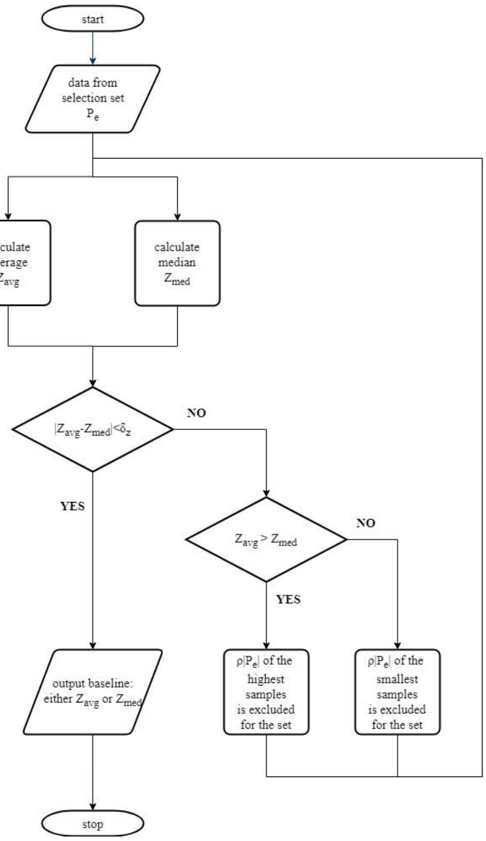

Fig. 3. The main procedures of the methods, averaging over the selection set and averaging over the flat chunk selection set, from [35].

Here, there are three methods: the average of the baseline dataset, median of the baseline dataset, and the iterative method. To evaluate performance, the baseline samples in the data used in the previous section were processed using these methods. The results of the baseline recoveries are shown in Figure 4. The discrete and continuous histograms are displayed using the median and average methods, respectively, because the data types for these two methods are "int" and "float." The histogram obtained using the iterative method is similar to that obtained using the median method. The only difference is the width of each discrete part, which is equal to twice the minimum difference parameter set in the algorithm(δ_z in Figure 3, here the value is 0.1, further details can be found in [35]). Gaussian functions were used to fit the envelopes of the three histograms; the results are listed in Table 1. Because the data are all integers for the median method, the most probable value(MPV) of the histogram is treated as zero and not the mean fitting parameter. From a comparison of the MPVs of the three methods, it can be concluded that all three methods are good estimators of the baseline levels, and therefore, fully meet the performance requirements

Algorithms subsequently become the focus of the selection criteria. The iterative method was the most complex of the

three methods. However, this method is powerful because it can continue to provide reasonable baseline values when the signal samples are also included the dataset [35]. The median method is simpler, albeit the data ranking algorithm is not "FPGA friendly." Therefore, for the CsI(Tl) array DAQ system, the average method is preferred.

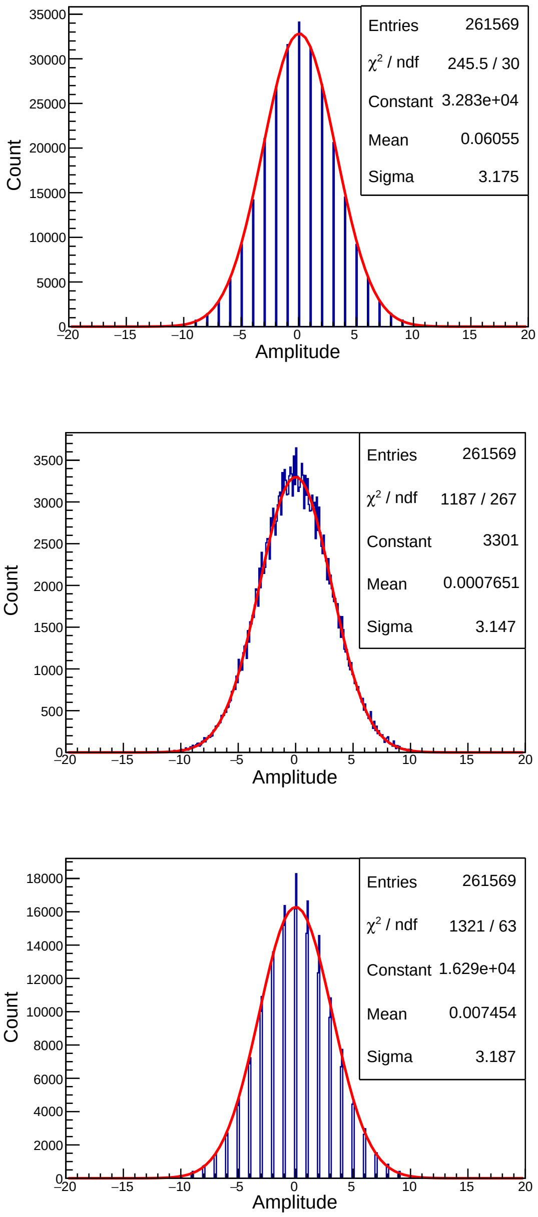

Fig. 4. Typical results of baseline restorations obtained with the following algorithms: (a) Median, (b) Average, and (c) Iteration.

TABLE 1. Fitting parameters of the three methods.

Methods	MPV	Sigma
Median	0	3.175
Average	0.0008	3.147
Iteration	0.007	3.187

C. Arrival time

According to the ETF design scheme, the CsI(Tl) array was intended to generate a trigger for the entire system. With the complete digitization of the input waveform and the powerful calculation capability of the FPGA, the CsI(Tl) array trigger signal can be generated and controlled by software. This simplifies the electronic system by eliminating the necessity for additional electronics, such as splitters and time discriminators.

An ETF trigger system consists of 2-level trigger generators [36]. At the front end, primary trigger signals were generated according to the signal shapes and logical relationships between the readout elements of a particular detector included in the trigger system. These primary trigger signals were subsequently fed into the global trigger logical unit to generate an event trigger signal for the entire system according to the physical interests. To improve logic operation effectiveness for signals with different delay times and time jitter, each primary trigger signal can be delayed and widened separately in a global trigger logical unit. From this perspective, time resolution is not the key element for the CsI(Tl) array.

Several methods are available to determine the arrival time of a signal. Common methods, which are identical to those in the analog scheme, are leading-edge discrimination (LED) and constant fraction discrimination(CFD). LED is the simplest method; however, it has a large time jitter owing to the time-walk effect. To achieve better performance, correction should be performed, which is a significant task for the FPGA programmer. Therefore, CFD was introduced to eliminate the time walk effect. There are two methods for implementing this algorithm in an FPGA: constant-fraction zero-crossing (CFDzc) and digital contact-fraction discrimination (dCFD) [37]. CFDzc is a digital version of the classic analog CFD [38], whereas dCFD is similar to an LED with a different threshold value, equal to the constant fraction of the signal amplitude [39]. Better performance in terms of time resolution was obtained with the CFDzc method than with the dCFD method [40]. Other methods exist for determining the arrival time of a signal, such as the RC-CR2 filter [41] and pulse-shape fitting. However, utilization of these algorithms is resource-intensive in the FPGA and considered outside the scope of this research.

Because time resolution is not the key criterion for the CsI(Tl) array, the LED method without interpolation was chosen to determine the arrival time, considering the expected high computational resource consumption of the energy extraction and PID procedures. Figure 5 shows the relationship between the amplitude of the waveform and arrival time using the previous data. The arrival time is the difference between

the reference time and the time when the first sample point is above the threshold. The time reference was selected as the point at which the ADC waveform passed through 90% of its full amplitude at the leading edge. Linear interpolation was used to reduce the reference time jitter. A clear dependency between the waveform amplitude and the arrival time is shown in Figure 5. Another phenomenon is that the lower the waveform amplitude , the greater the time jitter. This is because a low amplitude causes the leading edge of the waveform to become flat, and it is difficult to determine the time at which the waveform crosses the threshold and the time reference. Although the time jitter is as large as approximately 3 μs when the waveform amplitudes are extremely small, this may not be useful because a threshold can be set in the FPGA to determine the recorded signals. The time jitter of the waveforms with relatively large amplitudes was approximately 342ns(the σ value with a Gaussian fit).

Further analysis can be performed with time-walk correction, which was not implemented in the FPGA in the proposed scheme. A cubic polynomial, shown in Figure 5 with a red solid line, was used to fit the 2-dimension histogram. The arrival time histograms with and without time-walk correction are shown in Figure 6. Good correction can be obtained with small waveforms, and the time jitter is approximately 344 ns(the σ value with a Gaussian fit), which is almost identical the value obtained with large waveforms.

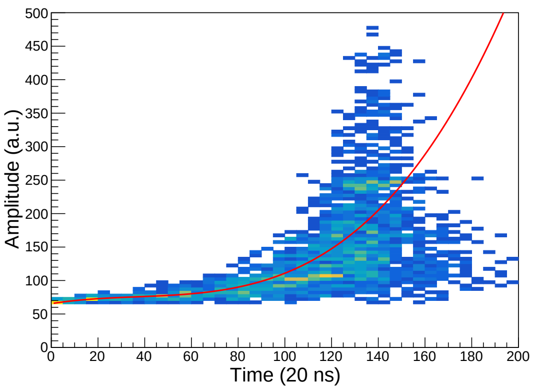

Fig. 5. The relationship between waveform amplitude and time obtained with LED method. Red line shows the fit result with a cubic polynomial, used to correct the time jitter.

D. Energy

In general, two quantities are used to extract the energy loss from the detector: the amplitude and total charge of the signal. These two quantities were measured using ADCs and charge-to-digital converters (QDCs) in a conventional DAQ system. Using a digital approach, these measurements are replaced by appropriate algorithms in the FPGA. However, the signal extracted from the CSA was too wide, indicating that the digital QDC method was not suitable for the CsI(Tl) array.

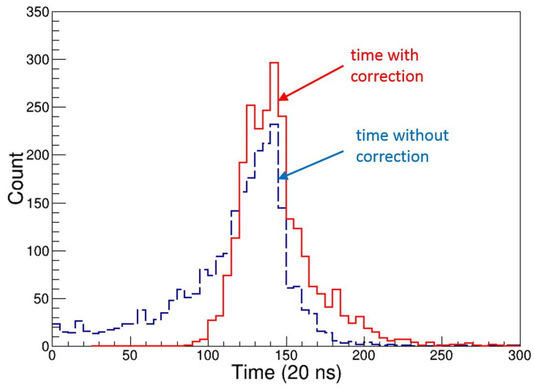

Fig. 6. (Color online) Time spectra obtained using LED technique. Blue dash line is the spectrum without time correction, red solid line is the spectrum with time correction.

The most direct approach to extract the signal amplitude is to determine the maximum(positive signal) or minimum(negative signal) waveform. However, the measured amplitudes were significantly influenced by noise. To improve the energy resolution, digital filters, which perform the same function as shaping amplifiers in an analog measurement system, were used to shape the signal before amplitude extraction. Theoretically, the best signal shape that maximizes the SNR is the infinite-width cusp [42]. However, a practical filter of this type is the finite-width cusp filter that limits the amplitude measurement of a single signal to a specific time. The algorithm uses a different function instead of an infinite exponential function and performs truncation [43, 44], which means that the performance is reduced. Other commonly used shaping filters include a series of trapezoidal [45–51] and CR-RC^m filters [52–54]. To identify a suitable shaping filter, the γ-rays produced by a ^{60}Co source were measured on a test bench operating in waveform mode, and the recorded data were processed with various digital filters. The waveforms before and after applying the shaping filters are shown in Figure 7. All parameters in each filter were optimized using repeated trials. The energy resolutions of the full-energy peaks for 1.33 MeV γrays were calculated as the criterion, and the results are shown in Table 2. The energy resolutions achieved by each filter were comparable with the performance of the finite cusp filter being slightly better. This is because the noise in the output test was extremely low, and the SNR values did not improve significantly. It should be noted that the noise level in the test is of the same order of magnitude as that of the ETF, indicating that all filters meet the requirements in terms of performance.

In [55], it is concluded that the family of trapezoidal filters offers good performance and simpler implementation among many other shaping filters, which influences this choice. Many algorithms exist for the implementation of trapezoidal filters, of which moving-window deconvolution (MWD) [49–51] is the simplest for FPGA implementation. Therefore, the MWD filter was selected as the shaping filter for the CsI(Tl) array, and the corresponding ^{60}Co energy

spectrum is indicated by the red dashed line in Figure 12.

E. PID algorithms

As previously mentioned, performing a pulse shape analysis for the CsI(Tl) array can reduce the background of charged particles in the energy spectrum of γ-rays and improve the PID performance through a combination with ΔE-E method. The basis of pulse shape analysis is that the ratio of the fast and slow components of light generated by the CsI(Tl) crystal depends on the type of incident particles, resulting in different shapes of the output waveform. Multiple methods exist for extracting these differences, among which the digital charge comparison [56–59] and rise-time comparison methods [59, 60] are widely used and straightforward to implement in the FPGA. Another method worth focusing on is called reconstructive particle identification (RPID) [51]. One reason is that this method was developed for CALIFA, whose construction is similar to the CsI(Tl) array. The RPID method can be successfully migrated into the DAQ system with significant potential. Another reason is that RPID can directly extract the fast and slow components of the CsI(Tl) crystal, thereby achieving a more improved performance.

To compare these PID algorithms, a triple α source (^{244}Cm, ^{239}Pu, and ^{241}Am) and a ^{60}Co source were used separately to irradiate the elemental detector of the CsI(Tl) array under identical conditions. The CsI(Tl) crystal envelope was pierced with a small hole to allow the α-particles to access the crystal. With respect to the digital charge comparison method, because the input signals are extracted from the CSA, which results in information on the incident particles being contained in the leading edges of the digitized waveforms, both time windows for charge integration were set to include the leading edge of the waveform with the same starting point, as shown in Figure 8. The starting point is determined using the dCFD method without interpolation. The integration windows size was determined through repeated trials. With respect to the rise-time comparison method, the rise time is defined as the time frame between the points where the waveforms cross 12.5 and 87.5% of the full amplitude in the leading edges. Because the method performance is correlated with the time accuracy, the linear interpolation technique was used to determine the cross-points. Regarding the RPID method, some parameters are identical to those of the MWD filter previously described, with three additional parameters: the fast and slow decay times of the CsI(Tl) crystal and the time window for the second MWD procedure. The fast and slow decay times are in accordance with [51], because they are almost constants. The length of the second time window was determined using repeated trials.

The two-dimensional PID spectra for each method are shown in Figure 9. Superficially, α and γ-rays were well identified for all three methods. The spectrum shown in Figure 9(a) illustrates that the rise time and the amplitude of the waveform are weakly correlated and can be considered independent. The red dashed lines in Figures. 9(b) and (c) indicate that the spectra approach zero when both the horizontal and vertical axes are reduced. These relationships indicate that the PID parameters listed in Table 3 can be used to convert two-dimensional spectra into one-dimensional histograms, and the figure-of-merit (FoM), as defined in [61, 62], can be used to quantify the separation performance of the PID methods. These one-dimensional histograms are shown in Figure 10 and the relevant FoMs are illustrated. Although data in the low-energy regions, which can make the FoM values larger than those in the beam experiments, were not included, the FoM values shown in Figure 10 remain good references for evaluating these three methods. Of the three methods, the rise time comparison achieved the worst score, which is consistent with the results in [28]. This is because the accuracy of the rise time deteriorated as the amplitude of the input signal decreased. Surprisingly, the RPID method does not work as well as the digital charge comparison method. One reason for this is the approximate treatments in the algorithm implementation process, such as calculating the exponential function. Moreover, it was identified that the decay time of the fast component in the CsI(Tl) array depends on the type of incident particles (more precisely, on the average energy density deposited in the crystal) [22, 63] and even on the total energy of the particles [20, 21], while the slow component decay time does not. If this is the case, RPID may not be an accurate method because of the underlying assumption of constant decay time. However, this remains sufficient for the separation of γ-rays and light-charged particles.

Overall, the aforementioned descriptions support the conclusion that the digital charge comparison method is preferred owing to its good performance and ease of FPGA implementation. Performance of the RPID method lags slightly; however, the complexity of this algorithm rules this option out. The rise-time comparison method had the worst performance among the three methods; however, the result remains acceptable, making it an alternative option to the digital charge comparison method.

IV. FINAL SCHEME AND PERFORMANCES OF DPP ALGORITHMS IN THE FPGA

Considering these aforementioned points, the final DPP algorithm scheme which includes a moving average filter, baseline restoration, leading-edge discrimination, moving window deconvolution, and digital charge comparison, is formed. Thus, the diagram in Figure 1 can be improved as shown in Figure 11. All DPP algorithms are "FPGA friendly," and further simplification can be achieved for the MAF and MWD by changing the algorithms to the recursive form. The algorithms were implemented in the DAQ system FPGA, completing the algorithm mode. The sampling rate was reset to 50 MS/s because the amount of data is significantly reduced. Subsequently, all procedures in Figure 11 are retested in this mode with the same radioactive sources used in Section III E. The energy spectra are shown in Figures. 12 and 13. A small shift can be observed between the two energy spectra of the ^{60}Co source compared to the result obtained in the raw waveform mode. This is because of the rounding operation

TABLE 2. The performances of different shaping filters.

Filters	Energy resolution (FWHM, 1.33MeV)	References
Cusp	5.58%	[43]
Trapezoidal (single exponential function)	5.74%	[47]
Trapezoidal (bi-exponential function)	5.85%	[47]
Trapezoidal (MWD)	5.67%	[51]
CRpz-RC2	5.70%	[53]
CRpz-RC4	5.79%	[53]

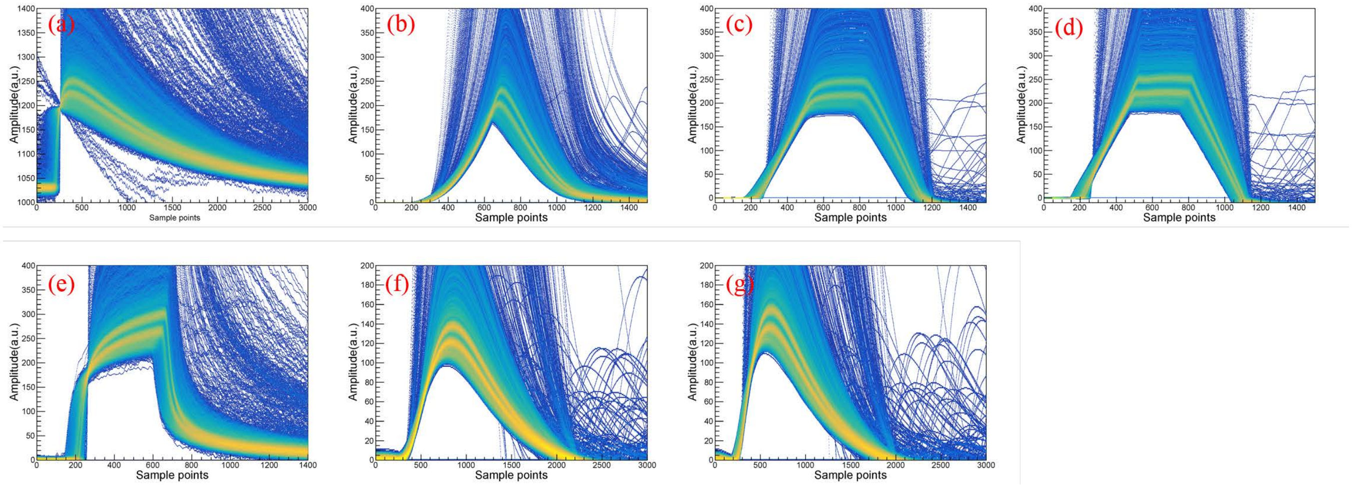

Fig. 7. (Color online) Shapes of raw waveform (a) and those modified by the following filters: (b) cusp, (c) trapezoidal with a single exponential function, (d) trapezoidal with a bi-exponential function, (e) MWD, (f) CRpz-RC2, and (g) CRpz-RC4.

TABLE 3. The PID functions for three PID methods.

Methods, Digital charge comparison, Rise-time comparison, and RPID	
PID functions	$PID = \frac{Q_s}{Q_l}$ $PID = t_{rise}$ $PID = \frac{N_f}{N_s}$

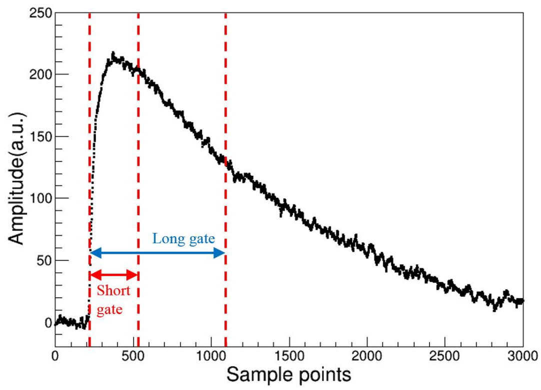

Fig. 8. Two integration windows in digital charge comparison method.

in the FPGA algorithm and changes in the DAQ system sampling frequencies. However, the energy resolutions for the 1.33 MeV full energy peak are almost unchanged.

The performance of the PID controller with the on-line algorithms is shown in Figure 14. Compared with the same results obtained from the raw waveform mode shown in Figure 10, almost the same positions where the peaks of the PID parameters are located can be found using the rise time and charge comparison methods. There is a slight improvement in the FoM parameter when comparing the charge comparison methods. This is owing to an improvement in the DAQ system sampling frequency. For the rise time method, the FoM parameter shows little differences. The reason for this is the rounding operation for the final result in the FPGA. Therefore, it can be concluded that only a minimal performance difference exists between the on-line and off-line DPP algorithms.

Table 4 lists the key performance metrics for the proposed algorithm. Good energy resolutions and PID performances are achieved, indicating that the on-line algorithms in the FPGA are well formed, and the final DPP algorithm scheme can adequately meets the requirements.

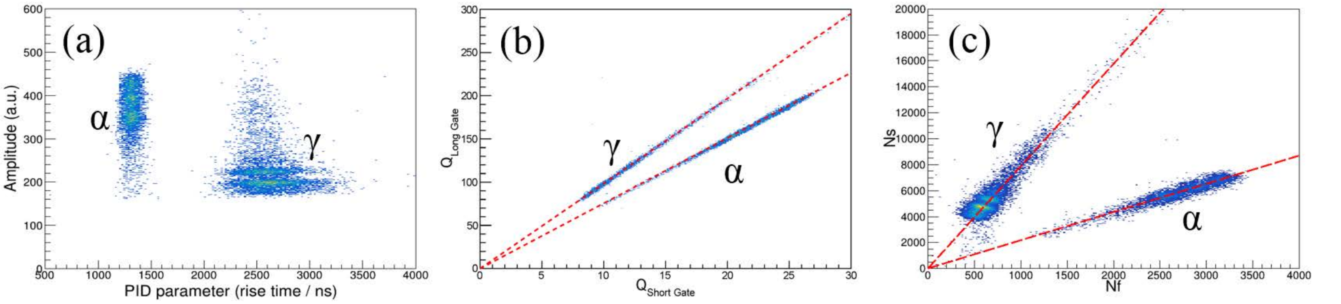

Fig. 9. 2-dimensions PID spectra for three methods: (a) rise-time comparison, (b) digital charge comparison, and (c) RPID. The $Q_{LongGate}$ and $Q_{ShortGate}$ are the two integral values in the long and short gates as shown in Figure 8. The N_s and N_f are the relative amplitude values of the slow and fast decay components of the CsI(Tl) crystal.Red dashed lines in (b) and (c) indicate that the spectra approach zero when both horizontal and vertical axis values are reduced. The rise-time comparison spectrum shows that rise time and amplitude of the waveform are weakly correlated and can be considered as independent. This indicates that the list of PID parameters in Table 3 is well defined owing to the nearly constant values of the PID parameters.

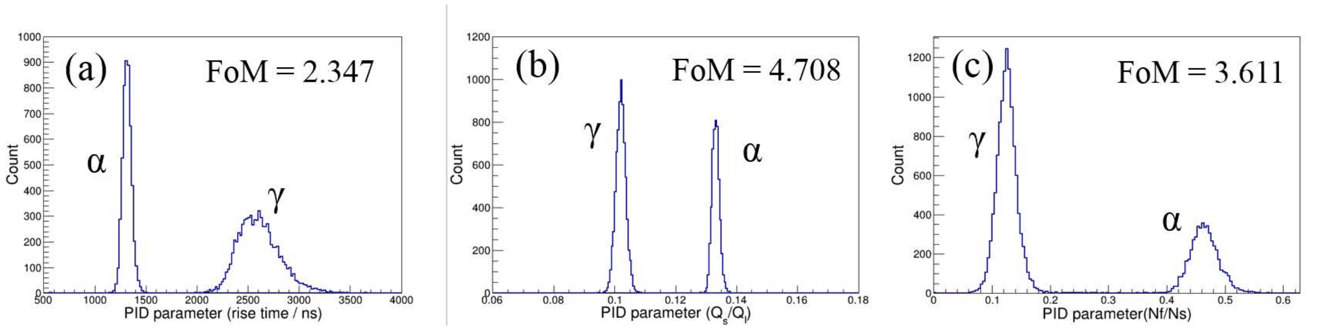

Fig. 10. Histograms of PID parameters including FoMs for three methods: (a) rise-time comparison, (b) digital charge comparison, and (c) RPID.

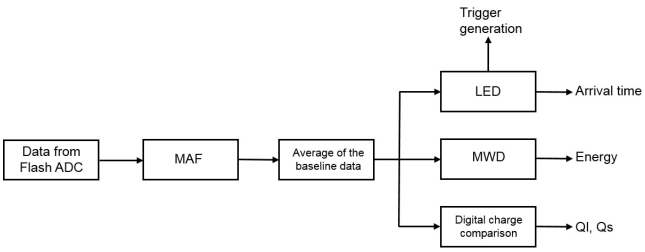

Fig. 11. Final DPP algorithm scheme in FPGA for the CsI(Tl) array at ETF.

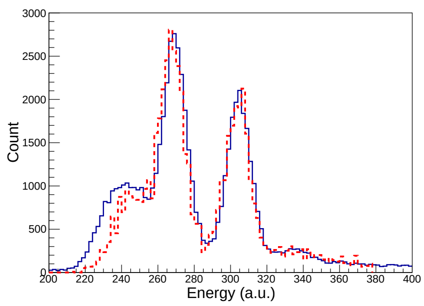

Fig. 12. (Color online) Energy spectra of ^{60}Co radioactive source. The histogram shown by the blue solid line is obtained by the DAQ system algorithm mode and the on-line MWD algorithm, while the histogram shown by the red dashed line is obtained by the raw waveform mode and the off-line MWD algorithm.

TABLE 4. Major parameters obtained from Figures 12, 13 and 14 by on-line algorithms.

Parameters	Quantities
energy resolution(1.17 MeV gamma-rays)	6.3%
energy resolution(1.33 MeV gamma-rays)	5.7%
energy resolution(5.16 MeV α ^{239}Pu)	10.4%
energy resolution(5.48 MeV α ^{241}Am)	7.8%
energy resolution(5.80 MeV α ^{244}Cm)	6.1%
FoM(digital charge comparison)	4.995
FoM(Rising time comparison)	2.329

V. SUMMARY

In this study, a scheme for DPP algorithms was developed for the CsI(Tl) array at ETF. A test bench with α and γ sources was constructed to determine the algorithms in each step, resulting in the following final scheme: moving

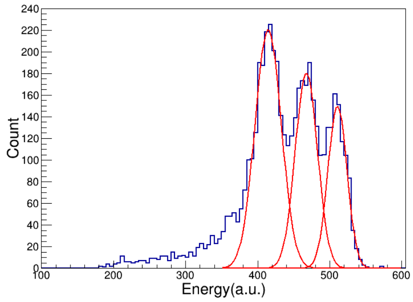

Fig. 13. (Color online) Triple α sources energy spectra obtained by the on-line MWD algorithm. A triple Gauss function, shown by the red line, is used to fit the peaks.

average filter, baseline restoration, leading-edge discrimination, moving window deconvolution, and digital charge comparison. Subsequently, the DAQ system algorithm mode is completed using these DPP algorithms. It was identified that the performance does not change significantly between on-line and off-line algorithms. With the algorithm mode, good performances in the energy spectrum and PID, as listed in Table 4, are achieved, which indicates that the proposed DPP algorithm scheme meets the requirements to upgrade the CsI(Tl)array DAQ system at the ETF of the HIRFL-CSR.

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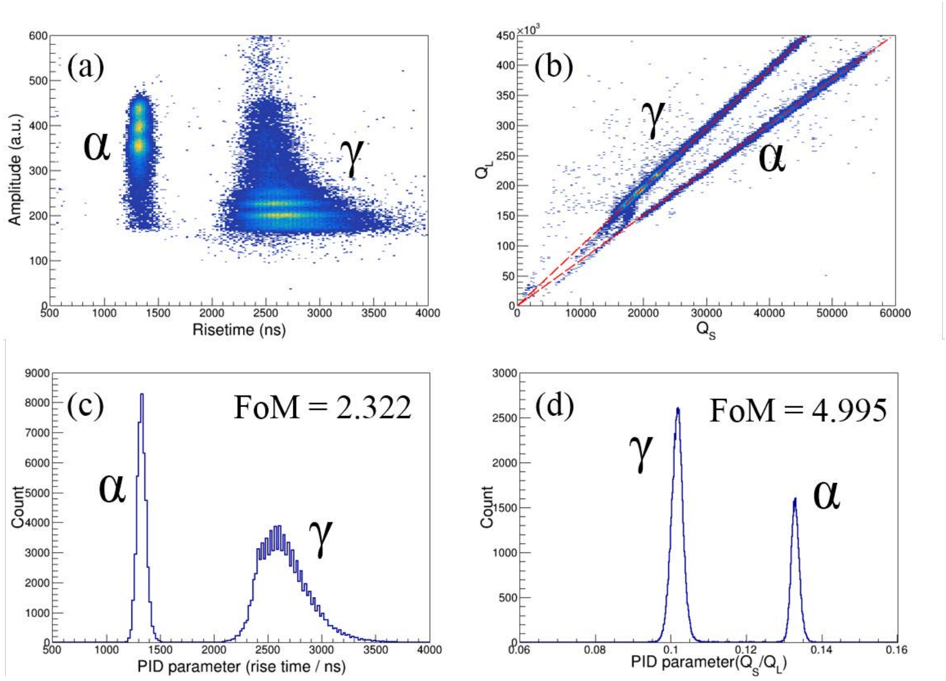

Fig. 14. On-line PID algorithm performance of digital charge comparison and rise-time comparison method in FPGA.

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